Chip back potential is the level which bulk silicon is maintained by on-chip connection, or it is the level to which the chip back must be connected when specifically stated below. If no potential is given the chip back should be isolated.

**PAD FUNCTIONS:**

1. **T CONT VLC**
2. **NOT I OUT**
3. **V-**
4. **I OUT**
5. **B1 MSB**
6. **B2**
7. **B3**
8. **B4**
9. **B5**
10. **B6**
11. **B7**
12. **B8 LSB**
13. **V+**
14. **VREF+**
15. **VREF-**
16. **COMP**

**.065”**

**.090”**

**3 2 1 16**

**15**

**14**

**13**

**12**

**4**

**5**

**6**

**7 8 9 10 11**

**DAC0800L B**

**MASK**

**REF**

**Top Material: Al**

**Backside Material: Si**

**Bond Pad Size: .0035” X .0035”**

**Backside Potential:**

**Mask Ref: DAC0800L B**

**APPROVED BY: DK DIE SIZE .065” X .090” DATE: 10/13/21**

**MFG: NATIONAL SEMI THICKNESS .013” P/N: DAC0800L**

**DG 10.1.2**

#### Rev B, 7/19/02